Notice of Allowability	Application No.	Applicant(s)	
	10/715,267	BROWN, NATHAN R.	
	Examiner	Art Unit	
	Sylvia R. MacArthur	1716	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *7/14/2010*.

2. ☒ The allowed claim(s) is/are *1,4-6,9-25 and 27-29*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John Farrell on 9/22/2010.

The application has been amended as follows:

16. (Currently Amended) A method for polishing at least one layer on a semiconductor device structure, comprising:

polishing at least one layer or a first semiconductor device structure;

locating any raised areas on the first semiconductor device structure following the polishing;

individually applying pressure by biasing rigid, independently movable pressurization structures to individually apply a plurality of different amounts of pressure to different, discrete locations of a backside of the semiconductor device structure, wherein biasing comprises magnetically biasing at least one of the rigid, independently movable pressurization structures against the backside of at least one second semiconductor device structure, the individually applying first semiconductor device structure, the individually applying being

effected at locations beneath areas of the at least one second semiconductor device structure that correspond to the raised areas of the first semiconductor device structure; and

at least mechanically polishing at least one layer of at least one second semiconductor device structure.

26. (Cancelled)

27. (Currently Amended) The method of claim ~~26~~16, wherein employing the magnet comprises repelling the at least one pressurization structure toward the backside to effect biasing.

28. (Currently Amended) The method of claim ~~26~~16, wherein employing the magnet comprises attracting the at least one pressurization structure toward the backside to effect biasing.

30-32. (Cancelled)

2. The following is an examiner's statement of reasons for allowance: The prior art of record fails to teach or fairly suggest a method of polishing or planarizing a surface of a semiconductor device structure, comprising magnetically biasing at least one of the rigid, independently movable pressurization structures against the backside of a semiconductor device structure as recited in claims 1 and 16.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sylvia R. MacArthur whose telephone number is 571-272-1438. The examiner can normally be reached on M-Th during the hours of 8 a.m. and 4:30 p.m..

5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 23, 2010

/Sylvia R MacArthur/
Primary Examiner, Art Unit 1716

IN THE CLAIMS

1. (Currently amended) A method for polishing or planarizing a surface of a semiconductor device structure, comprising:

biasing rigid, independently movable pressurization structures to individually apply a plurality of different amounts of pressure to different, discrete locations of a backside of the semiconductor device structure, wherein biasing comprises magnetically biasing at least one of the rigid, independently movable pressurization structures against the backside; and

polishing or planarizing at least one layer on the surface of the semiconductor device structure.

2. - 3. (Canceled)

4. (Previously presented) The method of claim 3, wherein magnetically biasing comprises magnetically repelling at least one of the rigid, independently movable pressurization structures toward the backside.

5. (Previously presented) The method of claim 3, wherein magnetically biasing comprises magnetically attracting at least one of the rigid, independently movable pressurization structures toward the backside.

6. (Previously presented) The method of claim1 wherein biasing further comprises resiliently biasing at least one of the rigid, independently movable pressurization structures against the backside.

7.-8. (Canceled)

9. (Previously presented) The method of claim 1, wherein polishing or planarizing comprises chemical-mechanical polishing.

10. (Previously presented) The method of claim 1, wherein biasing and polishing or planarizing together effect the formation of a substantially planar surface on the semiconductor device structure.

11. (Original) The method of claim 1, further comprising locating at least one raised area on an active surface of the semiconductor device structure.

12. (Previously presented) The method of claim 11, wherein biasing includes applying an appropriate amount of pressure to the backside of the semiconductor device structure, opposite the at least one raised area so as to planarize the active surface during the polishing or planarizing.

13. (Previously presented) The method of claim 11, wherein biasing includes individually applying pressure to a backside of another semiconductor device structure of the same type as the semiconductor device structure, opposite a location of the at least one raised area of the semiconductor device structure.

14. (Previously presented) The method of claim 13, wherein polishing or planarizing comprises forming a substantially planar surface on the another semiconductor device structure.

15. (Original) The method of claim 1, comprising
substantially simultaneously applying the plurality of different amounts of pressure to the backside of the semiconductor device structure.

16. (Currently Amended) A method for polishing at least
one layer on a semiconductor device structure, comprising:
polishing at least one layer or a first semiconductor
device structure;

locating any raised areas on the first semiconductor device structure following the polishing;

individually applying pressure by biasing rigid, independently movable pressurization structures to individually apply a plurality of different amounts of pressure to different, discrete locations of a backside of the semiconductor device structure, wherein biasing comprises magnetically biasing at least one of the rigid, independently movable pressurization structures against the backside of at least one second semiconductor device structure, the individually applying first semiconductor device structure, the individually applying being effected at locations beneath areas of the at least one second semiconductor device structure that correspond to the raised areas of the first semiconductor device structure; and

at least mechanically polishing at least one layer of at least one second semiconductor device structure.

17. (Previously presented) The method of claim 16, wherein locating comprises employing metrology techniques.

18. (Previously presented) The method of claim 16, wherein individually applying comprises applying a sufficient amount of pressure at each of the locations to form a substantially planar surface on the at least one second semiconductor device structure.

19. (Previously presented) The method of claim 16, wherein individually applying comprises individually applying different amounts of pressure at different ones of the locations.

20. (Previously presented) The method of claim 16, wherein individually applying comprises determining an appropriate amount of pressure to apply to each of the locations based on a height of each corresponding raised area.

21. (Previously presented) The method of claim 16, wherein individually applying comprises selectively applying pressure to the backside of the at least one second semiconductor device structure to at least one annular location.

22. (Previously presented) The method of claim 16, wherein polishing comprises mechanically polishing the at least one layer of the first semiconductor device structure.

23. (Previously presented) The method of claim 16, wherein polishing comprises chemical-mechanical polishing the at least one layer of the first semiconductor device structure.

24. (Previously presented) The method of claim 16, wherein at least mechanically polishing comprises chemical-mechanical polishing the at least one layer of the at least one second semiconductor device structure.

25. (Previously presented) The method of claim 16, wherein individually applying comprises biasing at least one rigid pressurization structure against the backside of the at least one second semiconductor device structure.

26. (Cancelled)

27. (Currently Amended) The method of claim ~~26~~16, wherein employing the magnet comprises repelling the at least one pressurization structure toward the backside to effect biasing.

28. (Currently Amended) The method of claim ~~26~~16, wherein employing the magnet comprises attracting the at least one pressurization structure toward the backside to effect biasing.

29. (Previously presented) The method of claim 25, wherein biasing comprises resiliently biasing the at least one pressurization structure against the backside.

30.- 32. (Cancelled)